Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Canceled)

2. (Currently Amended) The integrated circuit of claim ~~1~~5, wherein differential buffer is further configured to adjust a rise time of the ~~third~~ second signal.

3. (Currently Amended) The integrated circuit of claim ~~1~~5, wherein the finite state machine of the training circuit is configured to use a training pattern to vary the phase and amplitude characteristics of the differential buffer subsequent to a power-up or in response to a request.

4. (Currently Amended) The integrated circuit of claim ~~3~~5, wherein the differential buffer comprises a chain of buffer stages.

5. (Currently Amended) An integrated circuit, comprising:

a transmitter including a transmitter buffer input, wherein the transmitter is configured to transmit a first signal;

a receiver including a receiver buffer output;

a differential buffer coupled between the transmitter buffer input and the receiver buffer output, wherein the differential buffer is configured to accept a second signal from the transmitter buffer input and to adjust the second signal in phase and amplitude to reduce the first signal at the receiver buffer output; and

a training circuit configured to set phase and gain characteristics of the differential buffer by determination of which phase and amplitude characteristics reduce peak-to-

peak noise at the receiver buffer output in response to introduction of a training signal to the transmitter,~~The integrated circuit of claim 3,~~ and wherein the training circuit further comprises:

one or more analog-to-digital converters coupled between the finite state machine and the differential buffer; and

a peak detector coupled ~~between the finite state machine and~~to the receiver buffer output, and

~~wherein the~~a finite state machine coupled to the peak detector and ~~is~~ configured to vary the gain ~~and phase~~ characteristic~~s~~ of the differential buffer by reading a parameter from the peak detector, via the analog-to-digital converters, and is configured to set a value on the analog-to-digital converters to control one or more variable current sources of the differential buffer based, at least in part, on the read parameter.

6. (Currently Amended) The integrated circuit of claim ~~1~~5, wherein the differential buffer ~~has~~ includes a variable current source to enable control of the amplitude or phase characteristics of the differential buffer.

7. (Currently Amended) The integrated circuit of claim ~~1~~5, wherein the training circuit is configured to set a programmable or variable load of the differential buffer to set the amplitude or phase characteristics of the differential buffer.

8. (Currently Amended) The integrated circuit of claim ~~1~~5, wherein the differential buffer includes a coarse delay circuit, a fine delay circuit, an amplitude control circuit, and a rise-time control circuit, and wherein the training circuit is configured to control the coarse delay circuit, the fine delay circuit, the amplitude control circuit, and the rise-time control circuit to set the phase and amplitude characteristics of the differential buffer to adjust the ~~third~~ second signal in phase and amplitude and to cancel a signal echo component of ~~the~~ a ~~second~~ third signal at the receiver buffer output.

9. (Currently Amended) The integrated circuit of claim ~~1~~5, wherein the training circuit is configured to vary the phase and amplitude characteristics of the differential

buffer as part of a calibration procedure initiated following power-up or ~~after being initiated~~ on request.

10. (Canceled)

11. (Previously Presented) The integrated circuit of claim 8, wherein the coarse delay circuit comprises a digital delay line, a pair of multiplexers, and logic to control the multiplexers.

12. (Previously Presented) The integrated circuit of claim 11, wherein the digital delay line comprises a cascade of buffers.

13. (Previously Presented) The integrated circuit of claim 11, further comprising a pair of multiplexers configured to select signals from the digital delay line.

14. (Currently Amended) The integrated circuit of claim 11, wherein the training circuit is configured to generate control signals to be used to select signals from the digital delay line in the coarse delay circuit to vary a delay of the ~~third~~ second signal through the differential buffer.

15. (Canceled)

16. (Canceled)

17. (Currently Amended) The integrated circuit of claim ~~1~~5, ~~further comprising an analog-to-digital converter coupled to the training circuit,~~ wherein the one or more analog-to-digital converters ~~is~~ are configured to provide a control voltage to the differential buffer to vary ~~an~~ the amplitude of the ~~third~~ second signal.

18. (Previously Presented) The integrated circuit of claim 8, wherein the amplitude control circuit comprises a buffer with a variable load.

19. (Previously Presented) The integrated circuit of claim 18, wherein the training circuit is configured to control a gate voltage of an NMOS transistor to vary the variable load.

20. (Previously Presented) The integrated circuit of claim 8, wherein the rise-time control circuit comprises switches, capacitors, and control logic.

21. (Currently Amended) The integrated circuit of claim 8, wherein the training circuit is configured to generate control signals for the rise-time control circuit to vary a rise-time of the ~~third~~ second signal.

22. (Previously Presented) The integrated circuit of claim 5, wherein the peak detector comprises an amplitude cancellation sensor, a phase cancellation sensor, and an analog multiplexer.

23. (Currently Amended) The integrated circuit of claim 22, wherein the finite state machine is configured to adjust another amplitude and/or another phase characteristic of ~~the~~ another integrated circuit during a calibration phase.

24. (Previously Presented) The integrated circuit of claim 22, wherein the amplitude cancellation sensor comprises an integrator and a sample-and-hold device.

25. (Previously Presented) The integrated circuit of claim 22, wherein the phase cancellation sensor is configured to cycle through a reset phase, an integration phase, and a transfer phase during a calibration phase.

26. (Previously Presented) The integrated circuit of claim 25, wherein the finite state machine is configured to control timing of the reset, integration, and transfer phases.

27. (Previously Presented) The integrated circuit of claim 22, wherein the finite state machine is further configured to inject patterns into the transmitter and to measure a resulting offset in the amplitude cancellation sensor.

28. (Previously Presented) The integrated circuit of claim 22, wherein the phase cancellation sensor comprises a full-wave rectifier plus integrator and a sample-and-hold circuit.

29. (Previously Presented) The integrated circuit of claim 24, wherein the integrator is configured to cycle through a reset phase, an integration phase, and a transfer phase.

30. (Previously Presented) The integrated circuit of claim 28, wherein the finite state machine is configured to control timing of phases for the phase cancellation sensor.

31. (Canceled).

32. (Canceled)

33. (Canceled)

34. (Canceled)

35. (Currently Amended) A method for operating an integrated circuit~~The method of claim 39~~, ~~further~~ comprising:

transmitting a first signal from an output buffer of ~~the~~ a transmitter of the integrated circuit to another circuit, wherein the first signal is also coupled into an input buffer of ~~the~~ a receiver of the integrated circuit;

receiving a second signal from the other circuit;

transmitting a third signal from ~~the~~ an input buffer of the transmitter through ~~the~~ a differential buffer;

adjusting, via the differential buffer, the third signal in phase and amplitude; and

coupling the adjusted third signal into the output buffer of the receiver to cancel a signal echo component of the second signal~~.~~;

setting, by a training circuit, phase and gain characteristics of the differential buffer by determination of which phase and amplitude characteristics reduce peak-to-peak noise at the receiver buffer output in response to introduction of a training signal to the transmitter, wherein the setting further comprises:

varying phase and gain characteristics of the differential buffer by reading a parameter from a peak detector of the training circuit; and

setting a value on an analog-to-digital converters of the training circuit to control one or more variable current sources of the differential buffer based at least in part on the parameter.

36. (Previously Presented) The method of claim 35, wherein a third phase of the third signal is opposite to a first phase of the first signal.

37. (Previously Presented) The method of claim 35, wherein a third rise time of the third signal is adjusted to match a first rise time of the first signal.

38. (Currently Amended) The method of claim 35, wherein ~~a gain property of the differential buffer is varied, at least in part, by using~~the training signal comprises ~~the~~ a training pattern.

39. (Currently Amended) ~~A method for operating an integrated circuit, the~~The method of claim 38, ~~comprising~~wherein said setting further comprises:

~~applying, by a training circuit located on the integrated circuit, a training pattern to an input of a transmitter located on the integrated circuit;~~

varying a digital-to-analog code being applied to ~~a~~ the digital-to-analog converter ~~to adjust operating parameters of a differential buffer located on the integrated circuit~~;

measuring resulting noise conditions at an output buffer of ~~a~~ the ~~receiver located on the integrated circuit and coupled to an input buffer of the transmitter~~, wherein the noise conditions correspond to each applied digital-to-analog code;

determining a particular digital-to-analog code that corresponds to a reduced noise condition; and

applying the determined particular digital-to-analog code to the digital-to-analog converter ~~to calibrate the differential buffer~~.

40. (Canceled).

41. (Currently Amended) The integrated circuit of claim ~~1~~5, wherein the differential buffer is configured to ~~said~~ reduce the first signal at the receiver buffer output through a complete cancellation of the first signal at the receiver buffer output.

42. (Canceled)

43. (Currently Amended) The method of claim 39, wherein said reduced noise condition includes a minimized noise condition.

44. (Canceled)

45. (Currently Amended) The integrated circuit of claim [[44]]46, wherein the differential buffer is configured to ~~said~~ cancel the first signal at the receiver buffer output through a complete cancellation of the first signal at the receiver buffer output.

46. (Currently Amended) ~~The integrated circuit of claim 44, wherein the training circuit further comprises~~An integrated circuit, comprising:

a transmitter configured to transmit a first signal to another integrated circuit, wherein the transmitter has a transmitter buffer including a transmitter buffer output and a transmitter buffer input;

a receiver configured to receive a second signal from the other integrated circuit, wherein the receiver has a receiver buffer including a receiver buffer output and a receiver buffer input, and wherein the receiver buffer input is coupled to the transmitter buffer output;

a differential buffer coupled between the transmitter buffer input and the receiver buffer output, wherein the differential buffer is configured to accept a third signal from the transmitter buffer input and to adjust the third signal in phase and amplitude to cancel the first signal at the receiver buffer output; and

a training circuit, including a finite state machine located on the integrated circuit, configured to set phase and amplitude characteristics of the differential buffer by determination of which phase and amplitude characteristics minimize peak-to-peak noise at the receiver buffer output in response to introduction of a training signal to the transmitter;

wherein the training circuit further comprises:

one or more analog-to-digital converters coupled between the finite state machine and the differential buffer; and

a peak detector coupled between the finite state machine and the receiver buffer output, and

wherein the finite state machine is configured to vary gain and phase characteristics of the differential buffer by reading a parameter from the peak detector, via the analog-to-digital converters, and is configured to set a value on the analog-to-digital converters to control one or more variable current sources of the differential buffer based, at least in part, on the read parameter.